IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1.   (Cancelled).

2.   (Currently Amended) A system for ~~verification~~ verifying a design element of a system-on-a-chip (SOC) design, said system comprising:

said ~~system-on-a-chip (~~ an SOC[[)]] comprising:

said design element;

a master central processing unit (CPU) that ~~runs test case software~~ produces a first set of signals and a second set of signals for verifying said design element in response to running a verification case;

an SOC interface that receives said second set of signals; and

a first external bus interface unit (EBIU) that is slaved to said master CPU and receives said first set of signals; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification ~~interface model~~ logic device connected to said SOC interface; and

a second EBIU connected to said first EBIU and to said verification ~~interface model~~ logic device[[,]];

wherein said ~~test case software running on said master CPU controls both said SOC interface and said verification interface model~~ first set of signals received by said second EBIU is inputted to said verification logic device;

wherein said second set of signals received from said SOC interface is inputted to said verification logic device; and

wherein said verification logic device verifies said design element based on inputs from said first set of signals and said second set of signals.

3-7.   (Cancelled).

8.   (Currently Amended) A system for ~~verification~~ verifying a design element of a system-on-a-chip (SOC) design, said system comprising:

~~said system-on-a-chip (~~ an SOC[[)]] comprising:

said design element;

a master central processing unit (CPU) that ~~runs test case software~~ produces a first set of signals and a second set of signals for verifying said design element in response to signals produced by running a verification case;

an SOC interface that receives said second set of signals, said SOC interface ~~being~~ connected to said master CPU by a first internal bus; and

a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification ~~interface model~~ logic device connected to said SOC interface by a ~~first~~ second external bus; and

a second EBIU connected to said first EBIU by a ~~second~~ first external bus and to said verification ~~interface model~~ logic device by a third internal bus[[,]]

wherein said ~~test case software running on said master CPU controls both said SOC interface and said verification interface model~~ first set of signals received by said second EBIU is inputted to said verification logic device via said third internal bus;

wherein said second set of signals received from said SOC interface via said second external bus is inputted to said verification logic device; and

wherein said verification logic device verifies said design element based on inputs from said first set of signals and said second set of signals.

9.   (Currently Amended) The system in claim 8, ~~all the limitations of which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ comprises software drivers.

10.   (Currently Amended) The system in claim 8, ~~all the limitations of which are incorporated herein by reference,~~ wherein registers of said SOC interface and said verification ~~interface model~~ logic device are ~~programmed~~ controlled by the same ~~test~~ verification case ~~software~~.

11.   (Currently Amended) The system in claim 10, ~~all the limitations of which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ utilizes the same software driver to configure and control said SOC interface and said verification ~~interface model~~ logic device.

12.   (Currently Amended) The system in claim 10, ~~all the limitations of which are incorporated herein by reference,~~ wherein ~~said~~ verification test case ~~software~~ utilizes different software drivers to configure and control said SOC interface and said verification ~~interface model~~ logic device.

13.   (Currently Amended) The system in claim 8, ~~all the limitations of which are incorporated herein by reference,~~ wherein said verification ~~interface model~~ logic device tests an operational capability of said SOC interface.

14.   (Currently Amended) The system in claim 8, ~~all the limitations of which are incorporated herein by reference,~~ further comprising an additional verification ~~interface model~~ logic device for said verification test bench, said additional verification ~~interface model~~ logic device being connected to said second EBIU for testing additional types of SOC interfaces.

15.   (Currently Amended) A system for ~~verification~~ verifying a design element of a system-on-a-chip (SOC) design, said system comprising:
        ~~said system on a chip (~~ an SOC[[)]] comprising:
                said design element;

a master central processing unit (CPU) that ~~runs test case software~~ produces a first set of signals and a second set of signals for verifying said design element in response to signals produced by running a verification case;

an SOC interface that receives said second set of signals, said SOC interface being connected to said master CPU by a first internal bus; and

a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification ~~interface model~~ logic device connected to said SOC interface by a ~~first~~ second external bus; and

a second EBIU connected to said first EBIU by a ~~second~~ first external bus and to said verification ~~interface model~~ logic device by a third internal bus[[,]]

wherein said second EBIU and said first EBIU are mastered by said master CPU of said SOC, such that, said SOC interface and said verification ~~interface model are programmed by said test case software running on said master CPU~~ logic device receive said first set of signals and said second set of signals, respectively, as inputs based on the running of said verification case by said master CPU; and

wherein said verification logic device verifies said design element based on said inputs from said first set of signals and said second set of signals.

16.   (Currently Amended) The system in claim 15, ~~all the limitations of which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ comprises software drivers.

17.   (Currently Amended) The system in claim 15, ~~all the limitations of which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ utilizes the same software driver to configure and control said SOC interface and said verification ~~interface model~~ logic device.

18.   (Currently Amended) The system in claim 15, ~~all the limitations of which are incorporated herein by reference,~~ wherein ~~said~~ verification test case ~~software~~ utilizes different software drivers to configure and control said SOC interface and said verification ~~interface model~~ logic device.

19.   (Currently Amended) The system in claim 15, ~~all the limitations of which are incorporated herein by reference,~~ wherein said verification ~~interface model~~ logic device tests an operational capability of said SOC interface.

20.   (Currently Amended) The system in claim 15, ~~all the limitations of which are incorporated herein by reference,~~ further comprising an additional verification ~~interface model~~ logic device for said verification test bench, said additional verification ~~interface model~~ logic device being connected to said second EBIU for testing additional types of SOC interfaces.

21.   (Currently Amended) A method ~~of verification~~ for verifying a design element of a system-on-a-chip (SOC) design, said method comprising:
        producing a first set of signals and a second set of signals by a master central processing unit (CPU) of an SOC, which includes said design element, in response to running a verification case on said master CPU;
        slaving an SOC interface, which receives said second set of signals, and a first external bus interface unit (EBIU) of said SOC, which receives said first set of signals, to [[a]] said master CPU of said SOC;
        connecting said SOC interface to an external verification ~~interface model~~ logic device, which is external to said SOC;
        connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU ~~connecting~~ being connected to said external verification ~~interface model~~ logic device; [[and]]

~~controlling both said SOC interface of said SOC and said external verification interface model by test case software running on said master CPU of said SOC~~

inputting said first set of signals, received by said second EBIU, into said verification logic device;

inputting said second set of signals, received ~~by~~ from said SOC interface, into said verification logic device; and

verifying said design element based on inputs from said first set of signals and said second set of signals to said verification logic device.

22. (Currently Amended) The method in claim 21, ~~all the limitations of which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ comprises software drivers.

23. (Currently Amended) The method in claim 21, ~~all the limitations of which are incorporated herein by reference,~~ further comprising ~~programming~~ controlling registers of said SOC interface and said verification ~~interface model~~ logic device by the ~~same test~~ running of the verification case ~~software~~ on the master CPU.

24. (Currently Amended) The method in claim 23, ~~all the limitations of which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ utilizes the same software driver to configure and control said SOC interface and said verification ~~interface model~~ logic device.

25. (Currently Amended) The method in claim 23, ~~all the limitations of which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ utilizes different software drivers to configure and control said SOC interface and said verification ~~interface model~~ logic device.

26.   (Currently Amended) The method in claim 21, ~~all the limitations of which are incorporated herein by reference,~~ further comprising comparing said ~~SOC interface with said verification test interface~~ said first set of signals, received by said second EBIU, and inputted into said verification logic device and said second set of signals, received by from said SOC interface, and inputted into said verification logic device to test an operational capability of said SOC interface.

27.   (Currently Amended) The method in claim 21, ~~all the limitations of which are incorporated herein by reference,~~ further comprising:

connecting at least one additional verification ~~interface model~~ logic device to said second EBIU; and

testing additional types of SOC interfaces.

28.   (Currently Amended) A program storage device readable by machine tangibly embodying a program of instructions executable by the machine to perform a method for ~~verification~~ verifying a design element of a system-on-a-chip (SOC) design, said method comprising:

producing a first set of signals and a second set of signals by a master central processing unit (CPU) of an SOC, which includes said design element, in response to running a verification case on said master CPU;

slaving an SOC interface, which receives said second set of signals, and a first external bus interface unit (EBIU) of said SOC, which receives said first set of signals, to [[a]] said master CPU of said SOC;

connecting said SOC interface to an external verification ~~interface model~~ logic device, which is external to said SOC;

connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU ~~connecting~~ being connected to said external verification ~~interface model~~ logic device; [[and]]

~~controlling both said SOC interface of said SOC and said external verification interface~~ ~~model by test case software running on said master CPU of said SOC~~

inputting said first set of signals, received by said second EBIU, into said verification logic device;

inputting said second set of signals, received by from said SOC interface, into said verification logic device; and

verifying said design element based on inputs from said first set of signals and said second set of signals to said verification logic device.

29.   (Currently Amended) The program storage device in claim 28, ~~all the limitations of~~ ~~which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ comprises software drivers.

30.   (Currently Amended) The program storage device in claim 28, ~~all the limitations of~~ ~~which are incorporated herein by reference,~~ the method further comprising ~~programming~~ controlling registers of said SOC interface and said verification ~~interface model~~ logic device by the ~~same test~~ running of the verification case ~~software~~ on the master CPU.

31.   (Currently Amended) The program storage device in claim 30, ~~all the limitations of~~ ~~which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ utilizes the same software driver to configure and control said SOC interface and said verification ~~interface model~~ logic device.

32.   (Currently Amended) The program storage device in claim 30, ~~all the limitations of~~ ~~which are incorporated herein by reference,~~ wherein said ~~test~~ verification case ~~software~~ utilizes different software drivers to configure and control said SOC interface and said verification ~~interface model~~ logic device.

33.   (Currently Amended) The program storage device in claim 28, ~~all the limitations of~~ ~~which are incorporated herein by reference,~~ the method further comprising comparing said ~~SOC~~ ~~interface with said verification test interface~~ said first set of signals, received by said second EBIU, and inputted into said verification logic device and said second set of signals, received by from said SOC interface, and inputted into said verification logic device to test an operational capability of said SOC interface.

34.   (Currently Amended) The program storage device in claim 28, ~~all the limitations of~~ ~~which are incorporated herein by reference,~~ the method further comprising:

connecting at least one additional verification ~~interface model~~ logic device to said second EBIU; and

testing additional types of SOC interfaces.